



TFT MODULE SPECIFICATION

RVT50HQLNWCA0 V2.0A

IPS LVDS 5.0" LCD TFT DATASHEET
Rev. 1.0
2026-07-29

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ITEM	CONTENTS	UNIT
LCD Type	TFT/Transmissive/Normally black/IPS	/
Size	5.0	Inch
Viewing Direction	Free	/
Outside Dimensions (W x H x D)	120.70 x 75.80 x 5.65	mm
Active Area (W x H)	108.00 x 64.80	mm
Pixel Pitch (W x H)	0.135 x 0.135	mm
Resolution	800 (RGB) x 480	/
Brightness	800	cd/m ²
LCD Interface Type	LVDS	/
Color Depth	16.7 M	/
Pixel Arrangement	RGB Vertical Stripe	/
LCD Driver	ST7262	/
With/Without Touch	With Projected Capacitive Touch Panel	/
CTP IC	ILI2132A	/
LCD Input Voltage	3.3	V
Weight	TBD	g

Note 1. RoHS3 compliant

Note 2. LCM weight tolerance: ± 5%.

1. REVISION RECORD

REV NO.	REV DATE	CONTENTS	REMARKS
1.0	2026-07-29	Initial Release	

2. CONTENTS

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3. MODULE CLASSIFICATION INFORMATION

RV	T	50	H	Q	L	N	W	C	A0	V2.0A
1.	2.	3.	4.	5.	6.	7.	8.	9.	10.	11.

NO.	PARAMETER	SYMBOL
1.	BRAND	RV – Riverdi
2.	PRODUCT TYPE	T – TFT Standard
3.	DISPLAY SIZE	50 – 5.0”
4.	MODEL SERIAL NO.	H – High Brightness, IPS
5.	RESOLUTION	Q – 800 x 480 px
6.	INTERFACE	L – TFT LCD, LVDS
7.	FRAME	N – Without Mounting Metal Frame
8.	BACKLIGHT TYPE	W – LED White
9.	TOUCH PANEL	C – With Capacitive Touch Panel
10.	VERSION	A0 – αTouch
11.	MODULE REVISION	V2.0A

5. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Analog supply Voltage	VCI	-0.3	4.0	V	-
Backlight forward current	I _F	-	140	mA	For each serial LED
Operating Temperature	T _{OP}	-20	70	°C	-
Storage Temperature	T _{ST}	-30	80	°C	-

Note. The above are maximum values. If exceeded, they may cause permanent damage to the unit.

6. ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	REMARK
Digital supply Voltage	VDDI	3.0	3.3	3.6	V	
Input Signal Voltage	VIL	DGND	-	0.3*VDDI	V	RXIN0- ,RXIN0+,RXIN 1- ,RXIN1+,RXIN2- ,RXIN2+SELB,RES ET,STBYB,L/R,U/ D
	VIH	0.7*VDDI	-	VDDI	V	
Touch Panel Supply Current	ICTP	-	106	-	mA	Measured average current, touch panel active

7. TOUCH PANEL CHARACTERISTICS

PARAMETER	SYMBOL	VALUE	REMARK
Touch panel interface	-	I ² C	
I ² C 7-bit slave address	ADDR _{7-bit}	0x41	Standard I ² C address format
I ² C write address	ADDR _w	0x82	8-bit address format
I ² C read address	ADDR _r	0x83	8-bit address format

8. BACKLIGHT ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Backlight Driving Voltage	V _F	11.2	12	12.8	V	
Backlight Driving Current	I _F	-	140	-	mA	
Backlight Power Consumption	-	-	1680	-	mW	
Backlight Lifetime	-	-	50,000	-	hours	Note

Note: The “Operating lifetime” is defined as the module brightness decrease to 50% original brightness at Ta=25 °C and IF=140 mA. The LED lifetime could be decreased if operating IF is larger than 270 mA. Typical operating lifetime is estimated data.

9. ELECTRO-OPTICAL CHARACTERISTICS

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	RMK	NOTE
Response Time	Tr+Tf	$\theta=0^\circ$ $\phi=0^\circ$ Ta=25 °C	-	30	40	ms	FIG 1.	4, 7
Contrast Ratio	Cr		800	1000	-	---	FIG 2.	1, 7
Surface Luminance	Lv		-	800	-	cd/m2		2, 7
Luminance Uniformity	δ WHITE		75	80	-	%		3
Viewing Angle Range	θ	$\phi = 90^\circ$	70	80	-	deg	FIG 3.	6
		$\phi = 270^\circ$	70	80	-	deg		
		$\phi = 0^\circ$	70	80	-	deg		
		$\phi = 180^\circ$	70	80	-	deg		
CIE (x, y) Chromaticity	Rx	$\theta=0^\circ$ $\phi=0^\circ$ Ta=25 °C	0.554	0.584	0.614	-	FIG 2.	5,7
	Ry		0.320	0.350	0.380	-		
	Gx		0.335	0.365	0.395	-		
	Gy		0.542	0.572	0.602	-		
	Bx		0.125	0.155	0.185	-		
	By		0.085	0.115	0.145	-		
	Wx		0.285	0.315	0.345	-		
	Wy		0.311	0.341	0.371	-		
NTSC ratio	-	-	45	50	-	%		

Note 1. Contrast Ratio (CR) is defined mathematically as below, for more information see Figure 2.

$$\text{Contrast Ratio} = \frac{\text{Average Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}{\text{Average Surface Luminance with all black pixels (P1, P2, P3, P4, P5)}}$$

Note 2. Surface luminance is the LCD surface from the surface with all pixels displaying white. For more information see Figure 2.

L_v = Average Surface Luminance with all white pixels (P1, P2, P3, P4, P5)

Note 3. The uniformity in surface luminance δ WHITE is determined by measuring luminance at each test position 1 through 5, and then dividing the minimum luminance of 5 points luminance by maximum luminance of 5 points luminance. For more information see Figure 2.

$$\delta \text{ WHITE} = \frac{\text{Minimum Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}{\text{Maximum Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}$$

Note 4. Response time is the time required for the display to transition from white to black (Rise Time, T_r) and from black to white (Decay Time, T_f). For additional information see Figure 1. The test equipment is BM-7A.

Note 5. CIE (x, y) chromaticity, the x, y value is determined by measuring luminance at each test position 1 through 5, and then make average value.

Note 6. For TFT module, viewing angle is the angle at which the contrast ratio is greater 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to LCD surface. For more information see Figure 3.

Note 7. Viewing angle is measured at the center point of the LCD by CONOSCOPE (ergo-80). For response time testing, the testing data is based on BM-7A. Instruments for Contrast Ratio, Surface Luminance, Luminance Uniformity, Chromaticity the test data is based on SR-3A.

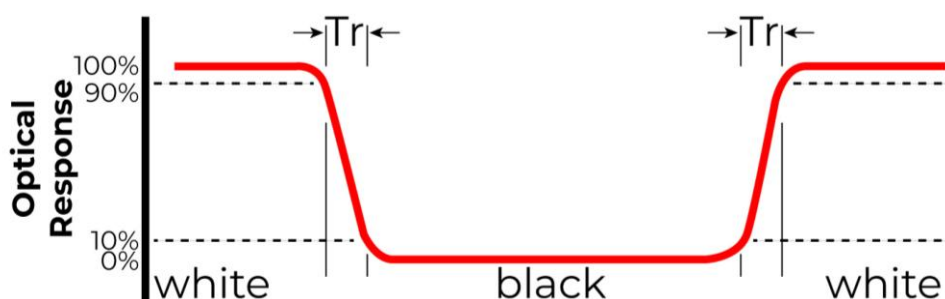


Figure 1. The definition of response time

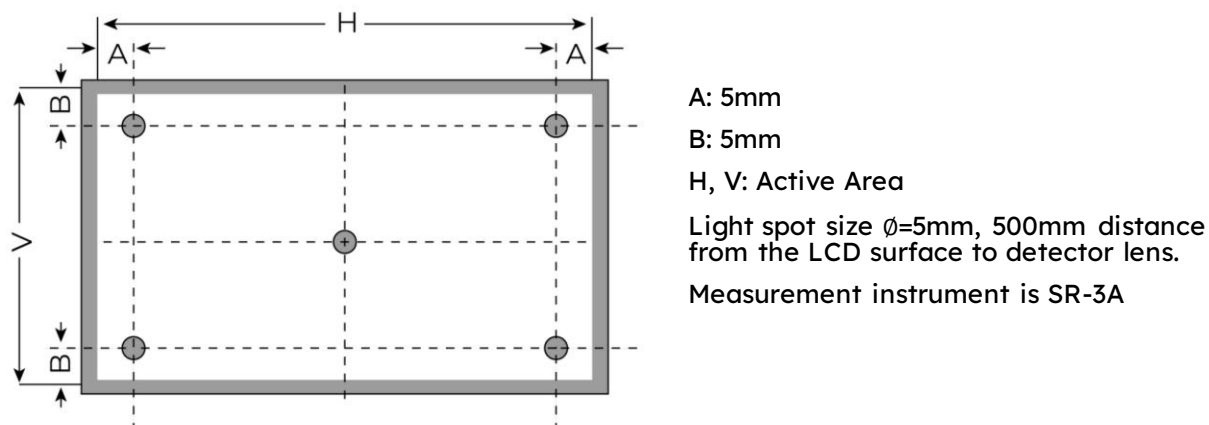


Figure 2. Measuring method for Contrast ratio, surface luminance, Luminance uniformity, CIE (x, y) chromaticity

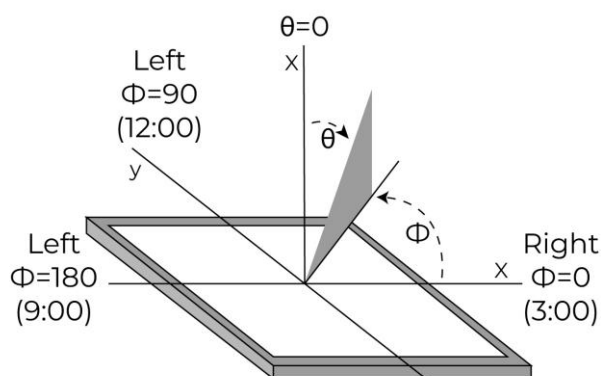


Figure 3. The definition of viewing angle

10. INTERFACES DESCRIPTION

10.1 TFT ASSIGNMENT

PIN	SYMBOL	I/O/P	DESCRIPTION
1	NC	-	No connection
2	VDD	P	Power voltage for digital circuit
3	VDD	P	Power voltage for digital circuit
4	NC	-	No connection
5	RESET	I	Global reset pin
6	STBYB	I	Standby mode, normally pulled high
7	GND	P	Ground
8	RXIN0-	I	-LVDS differential data input
9	RXIN0+	I	+LVDS differential data input
10	GND	P	Ground
11	RXIN1-	I	-LVDS differential data input
12	RXIN1+	I	+LVDS differential data input
13	GND	P	Ground
14	RXIN2-	I	-LVDS differential data input
15	RXIN2+	I	+LVDS differential data input
16	GND	P	Ground
17	RXCLKIN-	I	-LVDS differential clock input
18	RXCLKIN+	I	+LVDS differential clock input
19	GND	P	Ground
20	RXIN3-	I	-LVDS differential data input
21	RXIN3+	I	+LVDS differential data input

22	GND	P	Ground
23-24	NC	-	No connection
25	GND	P	Ground
26-27	NC	-	No connection
28	SELB	I	6-bit/8bit mode select
29	NC	-	No connection
30	GND	P	Ground
31-32	LED-	P	LED cathode
33	L/R	I	Horizontal inversion
34	U/D	I	Vertical inversion
35-38	NC	-	No connection
39-40	LED+	P	LED anode

I: input, P: Power

Note 1. Global reset pin. Active Low to enter Reset State. Normally pull high.

It's necessary to connecting with an RC delay circuit for stability.

(GRB delay VDD larger than 1ms)

Note 2. If LVDS input data is 6 bits, SELB must be set to High;
If LVDS input data is 8 bits, SELB must be set to Low.

Note 3. When L/R = "0", set right to left scan direction.
When L/R = "1", set left to right scan direction.
When U/D = "0", set top to bottom scan direction.

Note 4. U/D R/L Function description

SETTING OF SCAN CONTROL INPUT		SCANNING DIRECTION
U/D	L/R	
GND	DVDD	Up to down, left to right
DVDD	GND	Down to up, right to left
GND	GND	Up to down, right to left
DVDD	DVDD	Down to up, left to right

10.2 Touch Panel Connector

PIN	SYMBOL	DESCRIPTION
1	USB_GND	USB Ground
2	USB_VDD	USB Power for CTP, 5.0V
3	USB_D-	USB Data signal-
4	USB_D+	USB Data signal+
5	I2C_GND	I2C Ground
6	I2C_VDD	I2C Power for CTP 3.3V
7	I2C_RST	I2C Reset pin, active low
8	I2C_SCL	I2C Clock input
9	I2C_INT	I2C Interrupt signal from CTP, active low
10	I2C_SDA	I2C Data signal

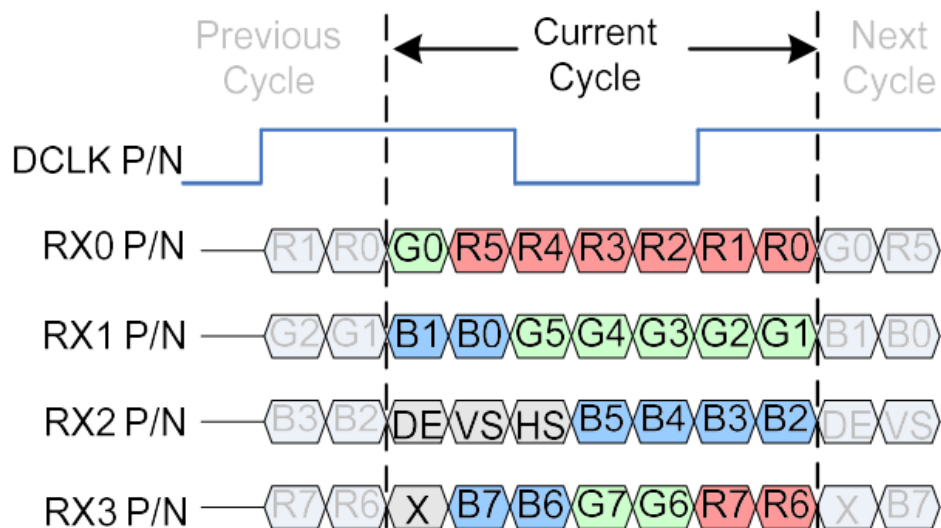
10.3 CN1 assignment

PIN	SYMBOL	DESCRIPTION
1	USB_VDD	USB_Power for CTP, DC 5.0V
2	USB_D-	USB_Data signal -
3	USB_D+	USB_Data signal +
4	USB_GND	USB_Ground

11. TIMING CHARACTERISTICS

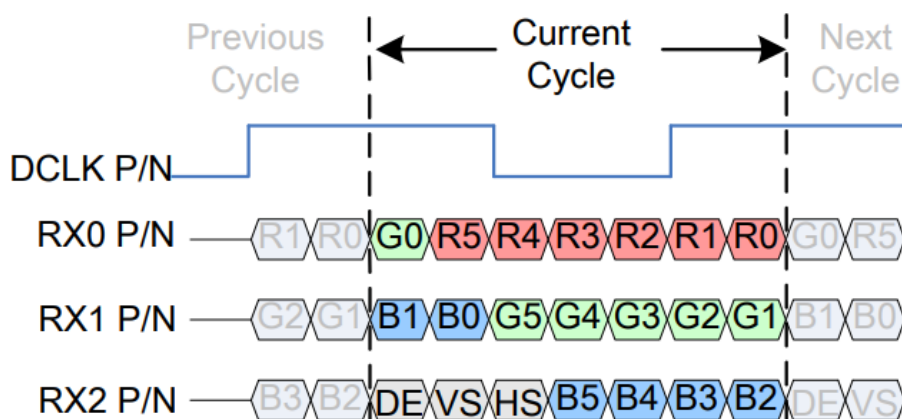
11.1 System bus timing for LVDS interface

11.1.1 4Lane VESA Data Format Color Bit Map



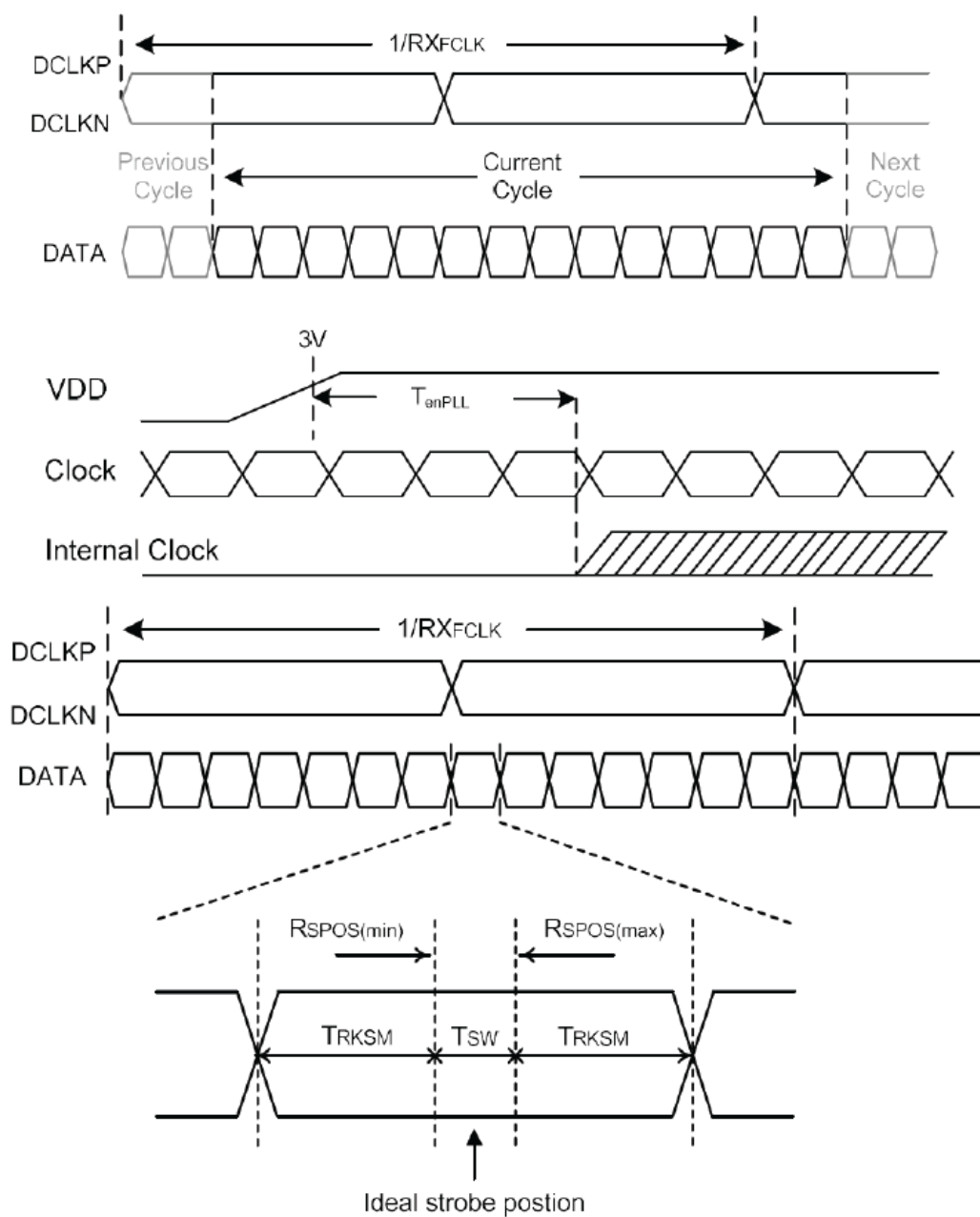
8-bit LVDS input mode, SELB='H'

11.1.2 3Lane VESA Data Format Color Bit Map



6-bit LVDS input mode, SELB='L'

11.1.3 LVDS Input Timing



R_{SKSM} : Receiver strobe margin

R_{SPOS} : Receiver strobe position

T_{SW} : Strobe width (internal DATA sampling window)

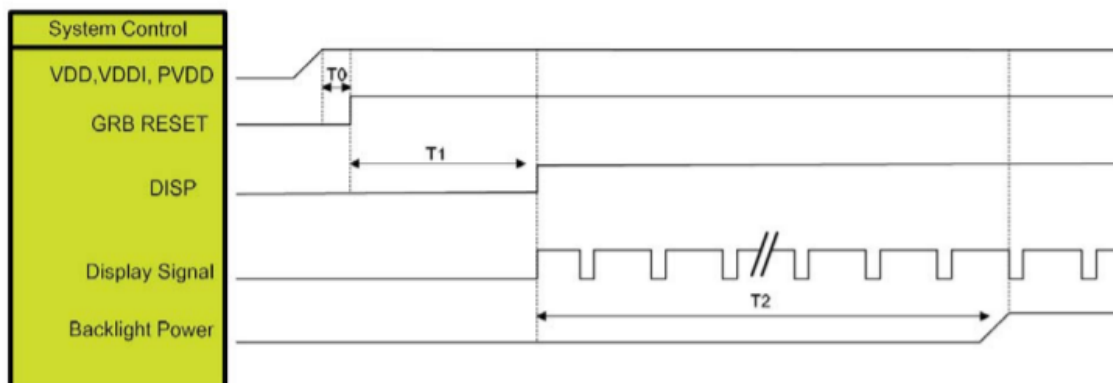
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Clock Frequency	RX_{FCLK}	23	25	27	MHz
Input Data Skew Margin	T_{RKSM}	400	-	-	ps
Clock High Time	T_{LVGH}	4/(7 x RX_{fclk})			ns
Clock Low Time	T_{LVGL}	3/(7 x RX_{fclk})			ns
PLL Wake-up Time	T_{enPLL}	-	-	150	μ s
LVDS Spread Spectrum Clocking (SSC) Tolerance of LVDS Receiver					
Modulation Frequency	SSC_{MF}	-	-	100	KHz
Modulation Rate	SSC_{MR}	-	-	± 3	%

11.2 Timing Table

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
DCLK frequency		Fclk	23	25	27	MHz
HSYNC	Period Time	Th	808	816	896	DCLK
	Display Period	Thdisp	800			
	H _{sync} Back Porch	Thbp	4	8	48	
	H _{sync} Front Porch	Thfp	4	8	48	
	H _{sync} Pulse Width	Thw	2	4	8	
VSYNC	Period Time	Tv	488	496	504	HSYNC
	Display Period	Tvdisp	480			
	V _{sync} Back Porch	Tvbp	4	8	12	
	V _{sync} Front Porch	Tvfp	4	8	12	
	V _{sync} Pulse Width	Tvw	2	4	8	

11.3 Power ON/OFF sequence

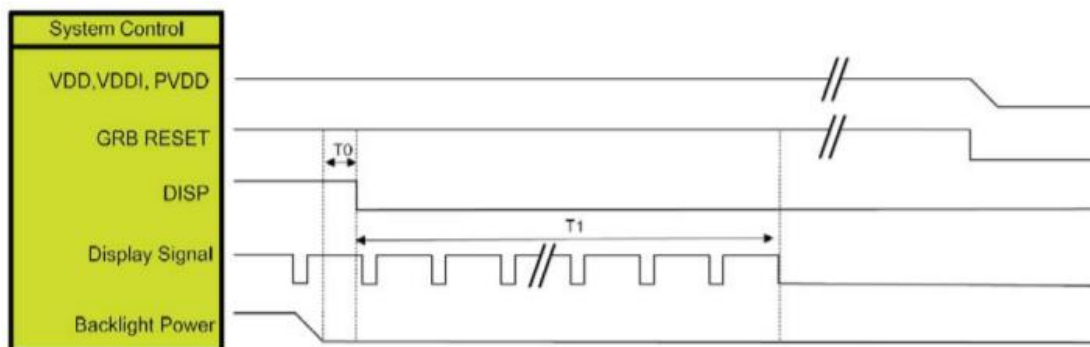
11.3.1 Power On sequence



SYMBOL	DESCRIPTION	MIN. TIME	UNIT
T0	System power stability to GRB RESET signal	0	ms
T1	GRB RESET=" High" to DISP=" High"	10	
T2	Display Signal output to Backlight Power on	250	

Note. LVDS interface Display signal: DCLK P/N; RX [3:0] P/N.

11.3.2 Power Off sequence



SYMBOL	DESCRIPTION	MIN. TIME	UNIT
T0	Backlight Power off to DISP="Low"	5	ms
T1	DISP="Low" to IC internal voltage discharge complete	100	

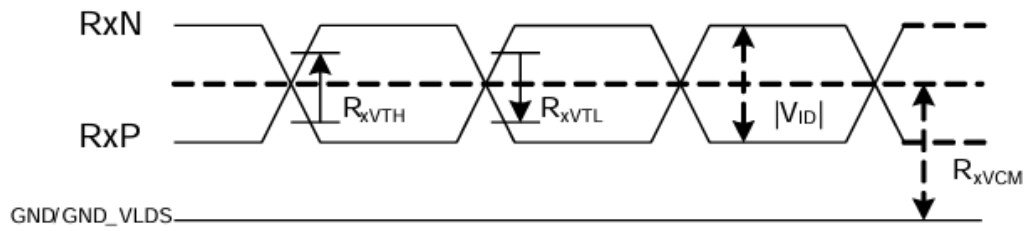
Note. LVDS interface Display signal: DCLK P/N; RX [3:0] P/N.

11.4 DC CHARACTERISTIC

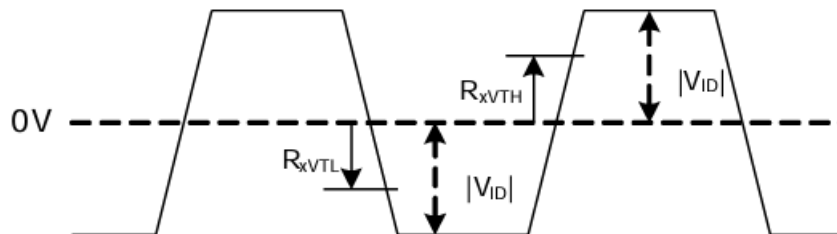
11.4.1 DC Characteristics for LVDS Receiver Circuit

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Differential Input High Threshold Voltage	R_{xVTH}	-	-	0.1	V	$R_{xVCM} = 1.2V$
Differential Input Low Threshold Voltage	R_{xVTL}	-0.1	-	-	V	
Input Voltage Range (Singled-End)	R_{xVIN}	0	-	VDD-1.0	V	
Differential Input Common Mode Voltage	R_{xVCM}	$ V_{ID} /2$	-	$2.4- V_{ID} /2$	V	
Differential Input Voltage	$ V_{ID} $	0.2	-	0.6	V	
Differential Input Leakage Current	RV_{xliz}	-10	-	10	uA	
LVDS Digital Operating Current	I_{VDD_LVDS}	-	10	15	mA	
LVDS Digital Stand-by Current	I_{STBD_LVDS}	-	10	50	uA	
Differential Input Termination Resistance	R_{ID}	90	100	110	Ω	

Single End Signals



Differential Signals



12. INSPECTION

Standard acceptance/rejection criteria for TFT module according to document available [here](#).

13. RELIABILITY TEST

NO.	TEST ITEM	TEST CONDITION	NOTE
1	High Temperature Storage	80°C/120 hours	A,B,C,D,E
2	Low Temperature Storage	-30°C/120 hours	
3	High Temperature Operating	70 °C /120 hours	
4	Low Temperature Operating	-20°C/120 hours	
5	High Temperature and High Humidity	+60°C , 90%RH, 120hrs	
6	Thermal Cycling Test (No operation)	-20°C/30 min ~ +70°C /30 min for a total 5 cycles, Start with cold temperature and end with high temperature.	A,B,C,D,E
7	Vibration Test	Sweep:10Hz~55Hz~10Hz 2G 2 hours for each direction of X. Y. Z. (6 hours for total)	A,B,C,D,E
8	Package Vibration Test	Random Vibration : 0.015G*G/Hz from 5-200HZ, -6dB/Octave from 200-500HZ 2 hours for each direction of X. Y. Z. (6 hours for total)	A,B,C,D,E
9	Package Drop Test	Height: 60 cm 1 corner, 3 edges, 6 surfaces	A,B,C,D,E
10	ESD	Contact=+/-4KV, Air=+/-8KV,(R=330R,C=150pF), 1 sec,9point,10times/point;	A,B,C,D,E

Notes

- A. LCM each function is OK.
- B. LCM appearance inspection without abnormalities (Including scratch, damage, corrosion and serious deformation)
- C. LCM brightness above the Min. value of Spec.
- D. Luminance uniformity above the Min. value of Spec.
- E. Color chromaticity within tolerance range.

14. LEGAL INFORMATION

CE marking is usually obligatory only for a complete end product. Riverdi display modules are semi-finished goods which are used as inputs to become part of the finished products.

Therefore, Riverdi display modules are not CE marked.

This is not a standalone product. It was designed as an electronic component. It needs integration with a whole system to be fully functional.

Riverdi grants the guarantee for the proper operation of the goods for a period of 12 months from the date of possession of the goods. If in a consequence of this guaranteed execution the customer has received the defects-free item as replacement for the defective item, the effectiveness period of this guarantee shall start anew from the moment the customer receives the defects-free item.

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We're here to ensure your project's success, every step of the way!